ABSTRACT OF THE DISCLOSURE

A content addressable memory (CAM) device having a plurality of CAM blocks and a block selection circuit. Each of the CAM blocks includes an array of CAM cells to store data words having a width determined according to a configuration value. The block selection circuit includes an input to receive a class code and circuitry to output a plurality of select signals to the plurality of CAM blocks. Each of the select signals selectively disables a respective one of the plurality of CAM blocks from participating in a compare operation according to whether the class code matches a class assignment of the CAM block.